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|  | **Department of Electronics & Communication Engineering** |  |  |
|  | **23CS311 – DIGITAL PRINCIPLES AND SYSTEM DESIGN** |  |  |
|  | **Third** |  |  |
| **QNo** | **PART A Questions** | **COs** | **Bloom’s Level** |
|  | Find the Octal equivalent of the hexadecimal number DC.BA. | CO1 | K1 |
|  | What is meant by multilevel gates networks? | CO1 | K1 |
|  | Discuss the NOR operation with a truth table. | CO1 | K2 |
|  | Write short notes on weighted binary codes. | CO1 | K1 |
|  | Convert (126)10 to Octal number and binary number. | CO1 | K2 |
|  | Prove the following using Demorgan’s theorem [(X+Y)’+(X+Y)’]’= X+Y | CO1 | K2 |
|  | Implement AND gate using only NOR gate | CO1 | K2 |
|  | State the principle of duality | CO1 | K2 |
|  | State and prove the consensus theorem. | CO1 | K2 |
|  | Realize XOR gate using only 4 NAND gates. | CO1 | K2 |
|  | What is the significance of BCD code. | CO1 | K1 |
|  | Convert a) (11001010)2 into gray code.  b) Convert a Gray code 11101101 into binary code. | CO1 | K2 |
|  | Describe the canonical forms of the Boolean function. | CO1 | K2 |
|  | What is a prime implicant? | CO1 | K1 |
|  | Define the following: minterm and maxterm? | CO1 | K1 |
| PART B | | | |
|  | Construct a combinational logic circuit to convert the Binary code to Gray code. (16) | CO1 | K3 |
|  | Solve the following switching functions using Karnaugh map method and realize expression using gates *F(A,B,C,D)* = *Σ(0,3,5,7,8,9,10,12,15).* (16) | CO1 | K3 |
|  | Solve and minimize the following expression using k-map  𝑌 = 𝐴̅𝐵𝐶̅𝐷̅ + 𝐴̅𝐵C + 𝐴𝐵𝐶̅𝐷̅ + 𝐴 𝐶̅𝐷̅ + 𝐴𝐵C (16) | CO1 | K3 |
| 1. 4 | (i) Build prime implicant and essential prime implicant. (3)  (ii) Develop the procedure for obtaining the logic diagram with NAND gates from a Boolean function with one example. (6)  (iii) Construct the switching function.  (𝑥, 𝑦, 𝑧) = ∑ 𝑚 (1,2,3,4,5,7) using K-Map. (7) | CO1 | K3 |
|  | Solve the following Boolean functions by using K-Map in SOP & POS. F (w, x, y, z) = ∑ 𝑚 (1, 3, 4, 6, 9, 11, 12, 14) (16) | CO1 | K3 |
|  | Solve and reduce the following function using K-map technique.  i) f (A, B, C) = ∑m (0,1,3,7) + ∑d (2,5) (8)  ii)F (w,x,y,z) = ∑m (0,7,8,9,10,12) + ∑d (2,5,13) (8) | CO1 | K3 |
| 1. 5 | i)Summarise and prove the De-morgan’s theorem. (5)  ii) Illustrate x + yz as the sum of minterms (3) | CO1 | K2 |
| 1. 6 | i) Outline the octal equivalent of hexadecimal numbers AB.CD (4)  ii) Demonstrate: a) Y = AB’D + AB’D’ b) Z = (A’+B)(A+B) (4) | CO1 | K2 |

**UNIT II**

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| **QNo** | **PART A Questions** | **COs** | **Bloom’s Level** |
|  | Define Combinational circuits. | CO2 | K1 |
|  | Draw the truth table of half adder. | CO2 | K2 |
|  | Write the Data flow description of a 4-bit Comparator. | CO2 | K1 |
|  | Implement a 4 bit even parity checker and generator. | CO3 | K2 |
|  | Implement a full adder with 4×1 multiplexer. | CO3 | K2 |
|  | Draw a 2 to 1 multiplexer circuit. | CO3 | K2 |
|  | What is priority encoder? | CO3 | K1 |
|  | Draw the truth table and circuit diagram of 4 to 2 encoder. | CO3 | K2 |
|  | Obtain the truth table for BCD to Excess-3 code converter. | CO3 | K2 |
|  | Distinguish between a decoder and a demultiplexer. | CO3 | K2 |
|  | Design a 2-bit binary to gray code converter. | CO3 | K2 |
|  | Distinguish between combinational logic and sequential logic. | CO2 | K2 |
|  | Implement half Adder using NAND Gates. | CO2 | K2 |
|  | Mention the different type of binary codes. | CO2 | K1 |
|  | Define logic synthesis and simulation. | CO3 | K1 |
| **PART B** | | | |
| 1. | Examine a combinational logic circuit to construct carry look ahead adder circuit with an example. (16) | CO2 | K4 |
|  | Analyse Octal to Binary Encoder and 3:8 Decoder with its truth table and implementation. (16) | CO3 | K4 |
|  | Analyze a brief note on the following combinational circuits:   1. Full adder (10) 2. Half subtractor (6) | CO2 | K4 |
|  | Analyse in detail about Magnitude comparator. (16) | CO2 | K4 |
|  | Analyze the concept of full subtractor circuit with truth table, Boolean expression and logic diagram. (16) | CO3 | K4 |
|  | Examine the concept of 4:1 multiplexer and 1:8 demultiplexer circuit in detail. (16) | CO3 | K4 |
|  | Simplify the function F = Σ (1,4,6,7,8,9,10,11,15) using 8 to 1 Multiplexer. (8) | CO2 | K4 |
|  | Examine a combinational logic circuit to construct BCD adder circuit with an example. (8) | CO3 | K4 |

**UNIT III**

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| **QNo** | **PART A Questions** | **COs** | **Bloom’s Level** |
|  | State the excitation table of JK Flip Flop. | CO4 | K1 |
|  | Write short notes on propagation delay. | CO4 | K1 |
|  | Give the block diagram of master-slave D flip- flop | CO4 | K2 |
|  | What is ring counter? | CO4 | K1 |
|  | With reference to a JK flip-flop, what is racing? | CO4 | K2 |
|  | What are Mealy and Moor machines? | CO4 | K1 |
|  | Write the characteristics table and equation of JK flip flop. | CO4 | K1 |
|  | Write any two applications of shift registers. | CO4 | K1 |
|  | Write the HDL code for up-down counter using behavioral model. | CO4 | K1 |
|  | Show D flip-flop implementation from a J-K flip-flop. | CO4 | K2 |
|  | Give the truth table for J-K flip-flop. | CO4 | K1 |
|  | Show the T-Flipflop implementation from SR flipflop. | CO4 | K2 |
|  | What is meant by triggering of Flip flop? | CO4 | K1 |
|  | What is a universal shift register? | CO4 | K1 |
|  | Give difference between latch and flip-flop. | CO4 | K2 |
| **Part – B** | | | |
|  | Analyze different types of shift register in detail using suitable diagram. (16) | CO4 | K4 |
|  | Analyze 3 bit synchronous up down counter using  K-map. (16) | CO4 | K4 |
|  | Examine a synchronous sequential circuit using D-flip flop to generates the following sequence and repeat 0,1,2,4,5,6. (16) | CO4 | K4 |
|  | Analyze a MOD-5 synchronous counter using T flip-flops. (16) | CO4 | K4 |
|  | Examine a synchronous counter that counts the sequence  1 – 3 – 15 – 5 – 8 – 2 – 0 - 12 – 6 – 9 using JK flip-flop. (16) | CO4 | K4 |
|  | Examine the operation of JK flip-flop and T flip-flop. (16) | CO4 | K4 |
|  | Examine the operation of Master slave JK flip-flop. (8) | CO4 | K4 |
|  | Analyze Modulo 6 asynchronous counter in detail. (8) | CO4 | K4 |

**Unit IV**

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| **Q.No** | **PART A Questions** | **CO’s** | **Bloom’s Level** |
| 1. | Define the critical race and non-critical race. | CO5 | K1 |
| 2. | What is lockout? How is avoided? | CO5 | K1 |
| 3. | What is critical race condition? Give example. | CO5 | K1 |
| 4. | Difference between synchronous and asynchronous sequential circuits | CO5 | K2 |
| 5. | What is a Hazard? | CO5 | K1 |
| 6. | Difference between fundamental mode circuits and pulse-mode circuits. | CO5 | K2 |
| 7. | What are cycles and races? | CO5 | K1 |
| 8. | What are the different types of shift type? | CO5 | K1 |
| 9. | What do you mean by Race condition? | CO5 | K1 |
| 10. | Differentiae Static & Dynamic Hazard | CO5 | K2 |
| 11. | What is ASM chart? | CO5 | K1 |
| 12. | What is State Assignment? | CO5 | K1 |
| 13. | Define Essential Hazard. | CO5 | K1 |
| 14. | Explain Multiple row method. | CO5 | K2 |
| 15. | Define closed covering. | CO5 | K1 |
| **Part - B** | | | |
| 1. | Develop an asynchronous sequential circuit that will output only the first pulse received. Any further pulses will be ignored. (16) | CO5 | K3 |
| 2. | Construct an asynchronous sequential circuit with 2 inputs and and one output Z with suitable example. (16) | CO5 | K3 |
| 3. | Construct a static and dynamic hazard free realization for the following function using   1. NAND Gates 2. NOR gate   F(a,b,c,d)= Σm (1,5,7,14,15). | CO5 | K3 |
| 4. | Develop the switching function F=Σm (1,3,5,7,8,9,14,15) by a static hazard free two level AND OR gate network. (16) | CO5 | K3 |
| 5. | Solve an asynchronous sequential circuit with 2 inputs D and G and with one output Z Wherever G is1, input D is transferred to Z. When G is 0; the output does not change for any change in D. Use SR latch for implementation of the circuit. (16) | CO5 | K3 |
| 6. | Construct an asynchronous sequential circuit whose output respond for every even numbered clock pulse. (16) | CO5 | K3 |
| 7. | Construct a circuit that has no static hazards and implement the Boolean function:  F(A,B,C,D)= Σm (0,2,6,7,8,10,12). (8) | CO5 | K3 |
| 8. | Build a hazard free realization for the following function Boolean function  F(A,B,C,D)= Σm (0,1,5,6,7,9,11). (8) | CO5 | K3 |

**UNIT V**

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| **QNo** | **PART A Questions** | **COs** | **Bloom’s Level** |
| 1. 1. | Write short notes on PLA. | CO6 | K1 |
| 1. 2. | Differentiate between EEPROM and PROM. | CO6 | K2 |
| 1. 3. | What is a volatile memory? Give example. | CO6 | K1 |
| 1. 4. | Distinguish between PAL and PLA. | CO6 | K2 |
| 1. 5. | Distinguish EEPROM and flash memory. | CO6 | K2 |
| 1. 6. | What is the difference between PROM and PLA? | CO6 | K1 |
| 1. 7. | What is PLA and Its uses? | CO6 | K1 |
| 1. 8. | What are the major drawbacks of the EEPROM? | CO6 | K1 |
| 1. 9. | Describe the basic functions of ROM and RAM. | CO6 | K2 |
|  | Give the different types of RAM. | CO6 | K1 |
|  | What is Memory refresh? | CO6 | K1 |
|  | What do you mean by PLD’s? | CO6 | K1 |
|  | Compare SRAM and DRAM. | CO6 | K2 |
|  | What is Configurable Logic Block? | CO6 | K1 |
|  | Distinguish between EPROM and EEPROM | CO6 | K2 |
| **Part – B** | | | |
| 1. | Explain the working of PAL and PLA with an example. (16) | CO6 | K2 |
| 1. 10. 2. | Infer a combinational circuit using ROM that accepts a three bit binary number and outputs a binary number equal to the square of the input number. (16) | CO6 | K2 |
| 1. 3. | Interpret the following function using PLA  A(x,y,z)= Σm(1,2,4,6) B(x,y,z)= Σm(0,1,6,7) C(x,y,z)= Σm(2,6) (16) | CO6 | K2 |
| 1. 4 | Outline a static RAM cell and dynamic RAM cell and explain its working. | CO6 | K2 |
| 1. 5. | Summarise a BCD to Excess-3 code converter and implement using suitable PLA. (16) | CO6 | K2 |
| 1. 6. | Explain any two error correction and error detection methods with an example. (16) | CO6 | K2 |
| 1. **7.** | Explain the following Boolean functions using PROM.  F1(x,y,z) = Σm (1,2,4,7) and F2(x,y,z) = Σm (3,5,6,7) (8) | CO6 | K2 |
| 1. 8. | Interpret the following Boolean functions using PLA with 3 inputs, 4 product terms and 2 outputs. F1(A,B,C) = Σm(3,5,6,7) and F2(A,B,C) = Σm (0,2,4,7) (8) | CO6 | K2 |